

# 128X128 CMOS PHOTODIODE-TYPE ACTIVE PIXEL SENSOR WITH ON-CHIP TIMING, CONTROL AND SIGNAL CHAIN ELECTRONICS

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## ABSTRACT

A 128x128 element CMOS active pixel image sensor (APS) with on-chip timing, control, and signal chain electronics has been designed, fabricated and tested. The chip is implemented in 1.2  $\mu\text{m}$  n-well process with a 19.2  $\mu\text{m}$  pixel pitch. The sensor uses a photodiode-type CMOS APS pixel with in-pixel source follower, row selection and reset transistors. The sensor operates from a +5 V supply and requires only a clock signal to produce video output. The chip performs correlated double sampling (CDS) to suppress pixel fixed pattern noise, and double delta sampling (DDS) to suppress column fixed pattern noise. The on-chip control circuitry allows asynchronous control of an inter frame delay to adjust pixel integration. On-chip control is also provided to select the readout of any size window of interest.

## 1. INTRODUCTION

For many imaging systems, integration of the image sensor with circuitry for both driving the image sensor and performing on-chip signal processing is becoming increasingly important. A high degree of electronics integration on the focal-plane can enable miniaturization of instrument systems and simplify system interfaces. In addition to good imaging performance with high quantum efficiency, low noise, no lag, no smear and good blooming control, it is desirable to have random access, simple clocks, low system power, simple power supplies and fast read out rates. The imaging chip described in this paper has demonstrated many of these capabilities.

The sensor uses active pixels, which denotes that active readout transistors are contained within each image pixel. This active pixel sensor (APS) technology has many advantages over CCDs<sup>1</sup>. In this implementation, the pixel contains a photodiode imaging element along with three transistors to perform the functions of readout, selection, and reset. A similar sensor was described in the late 1960's<sup>2</sup> and later developed as the Amplified MOS Imager<sup>3</sup>. In the JPL sensor, readout is achieved using a column parallel architecture which is multiplexed one row at a time and then one column at a time through a single on-chip amplifier/buffer. Digital circuits employ common logic elements to control row and address decoders and delay counters. The chip inputs that are required are a single +5 V power supply, start command, and parallel data load commands for defining integration time and windowing parameters. The output consists of two differential analog channels.

The CMOS APS chip reported here has performance suitable for many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics such as video phones, computer inputs and home surveillance devices. It has also been proposed for several scientific balloon applications as well as a radiation detector. Future development will lead to scientific sensors suitable for highly integrated imaging systems for NASA deep space and planetary spacecraft.

## 2. DESIGN AND OPERATION

A block diagram of the chip architecture is shown in figure 1. The analog outputs are VS\_OUT (signal) and VR\_OUT (reset), and the digital outputs are FRAME and READ. The inputs to the chip are asynchronous digital signals.

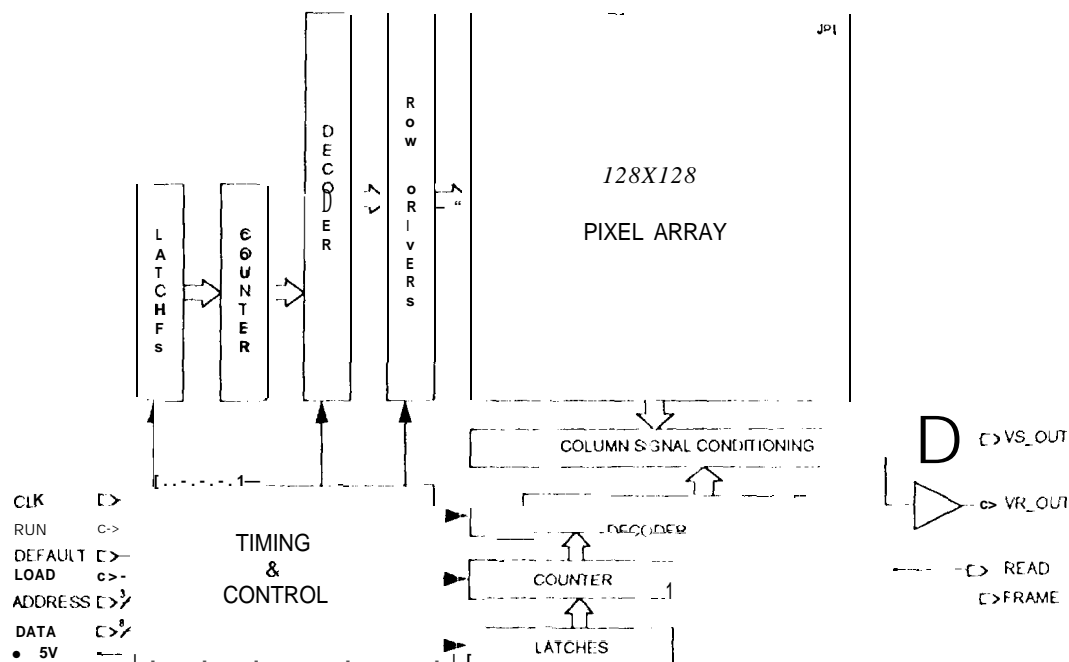


Figure 1. Block diagram of CMOS APS chip

The chip can be commanded to read out any area of interest within the 128x128 array. The decoder counters can be preset to start and stop at any value that has been loaded into the chip via the 8-bit data bus. An alternate loading command is provided using the DEFAULT input line. Activation of this line forces all counters to a readout window of 128x128.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the clock input frequency and is preset each frame from the latch and so can provide very large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time. A 30 Hz frame rate can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. This is the recommended time for setting the operating parameters. However, these parameters can be set at any time because of the asynchronous nature of operation. When RUN is activated, the chip begins continuous readout of frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion and then stops.

The CMOS APS, along with readout circuits, is shown schematically in fig. 2. The pixel unit cell consists of a photodiode (PD), a source-follower input transistor, a row-selection transistor and a reset transistor which controls lateral blooming through proper biasing of its gate. At the bottom of each column of pixels, there is a load transistor VIN and two output branches to store the reset and signal levels. Each branch consists of a sample and hold capacitor (CS or CR) with a sampling switch (SHS or S1 IR) and a second source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed pattern noise (not kTC noise) from the pixel. A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the

second SC( of source followers(VLP) and the subsequent clamp circuits and output source followers are common to the entire array.

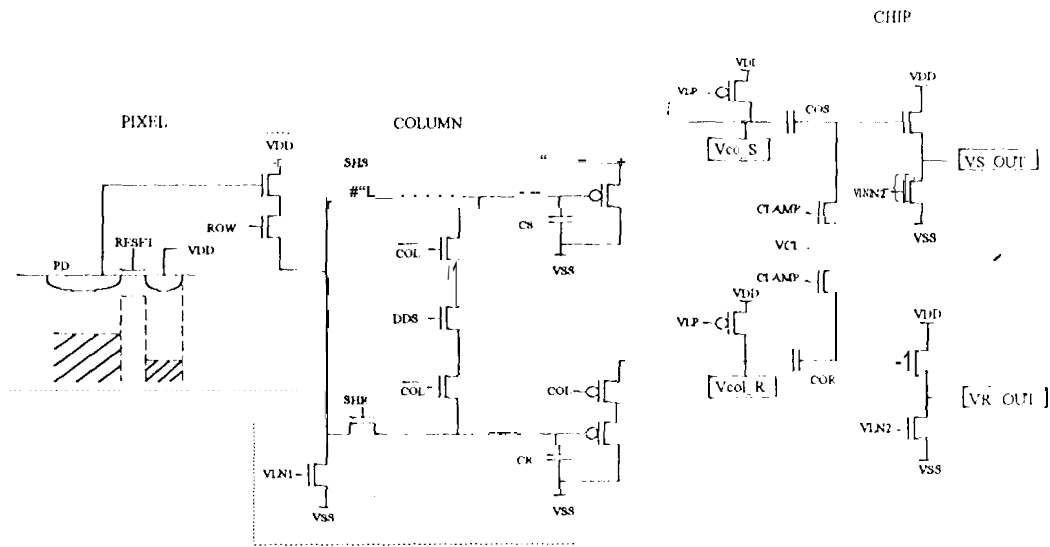


Figure 2. Schematic of active pixel sensor unit cell and readout circuitry

Timing for the readout sequence is shown in fig. 3. After a row has been selected, the signal that is present on each column pixel in that row is sampled (SHS) onto the holding capacitor CS. Next, each pixel in the row is reset (RESF1). This is followed by sampling the reset level (SHR) onto holding capacitor CR. A simplified expression for the output voltage of the reset branch of the column circuit is given by:

$$V_{col\_R} \cong \beta \{ \alpha [V_{pdr} - V_{tpix}] - V_{tcolr} \}$$

where  $\alpha$  is the gain of the pixel source-follower,  $\beta$  is the gain of the column source-follower,  $V_{pdr}$  is the voltage on the photodiode after reset,  $V_{tpix}$  is the threshold voltage of the pixel source-follower n-channel transistor, and  $V_{tcolr}$  is the threshold voltage of the column source-follower p-channel transistor. Similarly, the output voltage of the signal branch of the column circuit is given by:

$$V_{col\_S} \cong \beta \{ \alpha [V_{pds} - V_{tpix}] - V_{tcols} \}$$

where  $V_{pds}$  is the voltage on the photodiode with the signal charge present and  $V_{tcols}$  is the threshold voltage of the column source-follower p-channel transistor. Experimentally, the peak to peak variation in  $V_{tcolr} - V_{tcols}$  is typically 10-20 mV. It is desirable to remove this source of column-to-column fixed pattern noise FPN. JPL has previously developed a double delta sampling (DDS) technique to eliminate the column-to-column FPN<sup>4</sup>. This approach represents an improved version of the DDS circuitry.

Sequential readout of each column is as follows. First a column is selected. After a settling time equivalent 10 one-half the column selection period, the DDS is performed to remove column fixed pattern noise. In this operation, a DDS switch and two column selection switches on either side are used to short the two sample and hold capacitors CS and CR. Prior to the DDS operation the reset and signal column outputs ( $V_{col\_R}$  and  $V_{col\_S}$ ) contain their respective signal values plus a source follower voltage threshold component. The DDS switch is activated immediately after CLAMP is turned off. The result is a difference voltage coupled to the output drivers ( $VR\_OUT$  and  $VS\_OUT$ ) that is free of the voltage threshold component. Prior to CLAMP being deactivated, the output signals are:

$$VR\_OUT \cong \gamma (V_{cl} - V_{tr})$$

$$\text{and } V_{S\_OUT} \cong \gamma(V_{cl} - V_{ts})$$

where  $\gamma$  is the gain of the third stage source-follower,  $V_{cl}$  is the clamp voltage, and  $V_{tr}$  and  $V_{ts}$  are the threshold voltages of the third stage source-follower n-channel transistors, reset and signal branch respectively. Deactivation of the clamp circuit and simultaneous activation of the DDS switch causes several changes. The voltages in the two column branch sampling circuits equalize becoming:

$$V_{cs} = V_{cr} + \alpha[V_{pdr} - V_{tpix} + V_{pds} - V_{tpix}] / 2$$

This in turn causes a change in  $V_{col\_S}$  and  $V_{col\_R}$  to:

$$\begin{aligned} V_{col\_R}' &\cong \beta \{ \alpha [V_{pdr} - V_{tpix} + V_{pds} - V_{tpix}] / 2 - V_{teolr} \} \\ \text{and } V_{col\_S}' &\cong \beta \{ \alpha [V_{pdr} - V_{tpix} + V_{pds} - V_{tpix}] / 2 - V_{teols} \} \end{aligned}$$

Consequently, the voltage outputs change to:

$$\begin{aligned} V_{R\_OUT} &\cong \gamma(V_{cl} + V_{col\_R}' - V_{col\_R} - V_{tr}) \\ \text{and } V_{S\_OUT} &\cong \gamma(V_{cl} + V_{col\_S}' - V_{col\_S} - V_{ts}) \end{aligned}$$

We note

$$\begin{aligned} V_{col\_S}' - V_{col\_S} &= \beta \{ \alpha [V_{pds} - V_{pdr}] / 2 \} \\ \text{and } V_{col\_R}' - V_{col\_R} &= \beta \{ \alpha [V_{pdr} - V_{pds}] / 2 \} \end{aligned}$$

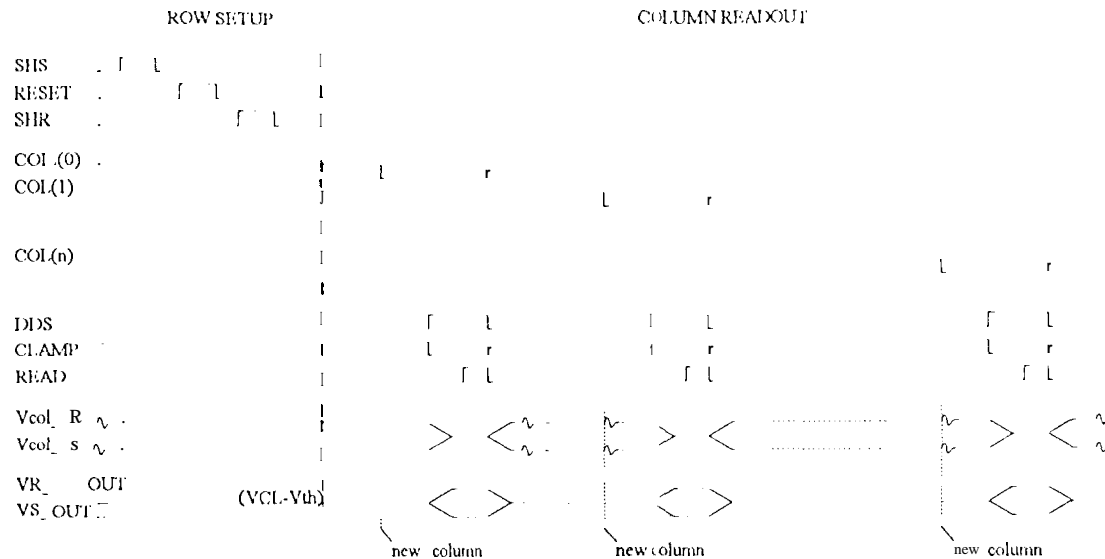


Figure 3. Timing diagram for setup and readout

When the outputs are differentially amplified off-chip, the common clamp voltage  $V_{cl}$  is removed, leaving only the difference between signal and reset. The net differential output voltage is given by:

$$V_{R\_OUT} - V_{S\_OUT} = \alpha \beta \gamma (V_{pdr} - V_{pds} - V_{const})$$

where  $V_{\text{const}}$  is a constant d.c. level.

A read signal is provided at the end of the DDS period to indicate that the signal outputs have settled and are ready for reading.

### 3. EXPERIMENTAL RESULTS

The chip was processed through MOSIS in the HP 1.2  $\mu\text{m}$  linear capacitor process and functioned as designed on first silicon. Capacitance values for the sample and hold capacitors (CR & CS) are typically 4 pF, while the output coupling capacitors (COR & COS) are approximately 14 pF. The yield based on 21 parts was quite good with only five parts having defective pixel sites. Only one part was non functional.

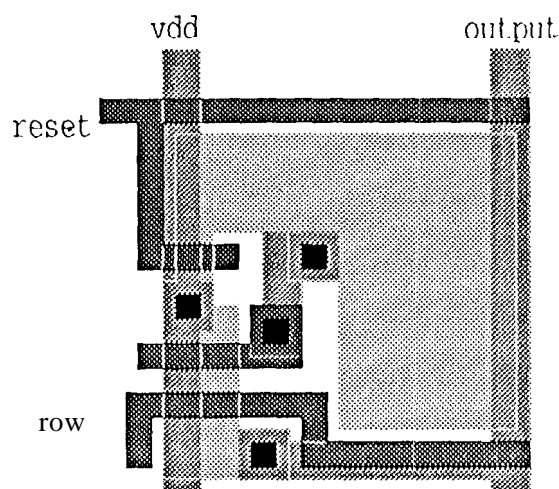


Figure 4. Layout of pixel. Fill factor is 30%.

Figure 4 shows the layout of the 19.2  $\mu\text{m}$  pixel unit cell. Row and reset are routed horizontally in polysilicon while the pixel output is routed in metal1. Metal2 was used as a light shield and covers most of the active area outside of the pixel array. The defined fill factor of the pixel was approximately 30%. Figure 5 shows a photograph of the chip with the various functional elements delineated.

Table 1. Design Characteristics

Array Size	128x128
Pixel Size	19.2 $\mu\text{m}$
Technology	1.2 $\mu\text{m}$ n-well CMOS (11 $\mu$ )
Maximum Clock Rate	10 MHz
Minimum Clock Rate	none
Maximum Pixel Rate	2.5 MHz
Maximum Integration Delay	$16 \times 10^9$ clock periods or 1600 secs at 10 MHz

Performance was measured for a broad range of parameters. These results are shown in table 2. A sample image produced for a 128x128 window is shown in fig. 6. The logo displayed in the upper left corner is a result of using metal2 as a light shield to block out the underlying pixels in the array.

The output saturation level of the sensor is 1.3 V when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the photodiode (perhaps 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8 volts). This corresponds to a full well of approximately 370,000 electrons. This can be increased by operating at a larger supply voltage, gaining perhaps 120,000 e- per supply volt.

Dark current was measured by varying the master clock rate and thus linearly controlling the integration period in the dark. An output-referred, room temperature, dark-current-induced-signal of 15  $\mu\text{V}/\text{sec}$  was measured, and good linearity was observed. Based on the conversion gain, this yields a dark current of less than 200 pA/cm<sup>2</sup>.

Conversion gain ( $\mu\text{V}/\text{e-}$ ) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1% similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer amplifier. Output-referred conversion gain was measured to be 3.5  $\mu\text{V}/\text{e-}$ , which is in reasonable agreement with the estimated photodiode and parasitic capacitance.

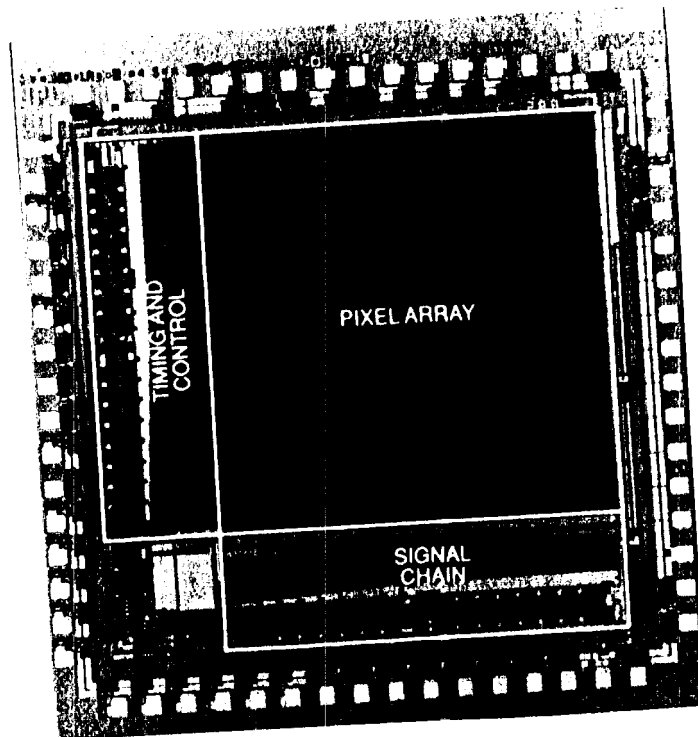


Figure 5. Photograph of completed CMOS APS IC.

The chip was also measured at 3 V supply voltage. The saturation level dropped to approximately 500 mV. The output-referred dark current signal in the sensor reduced to approximately 5 mV/sec, and the conversion gain remained approximately constant at 3.5  $\mu\text{V}/e^-$ . At 30 Hz frame rate operation, the chip dissipated 13.8 mW.

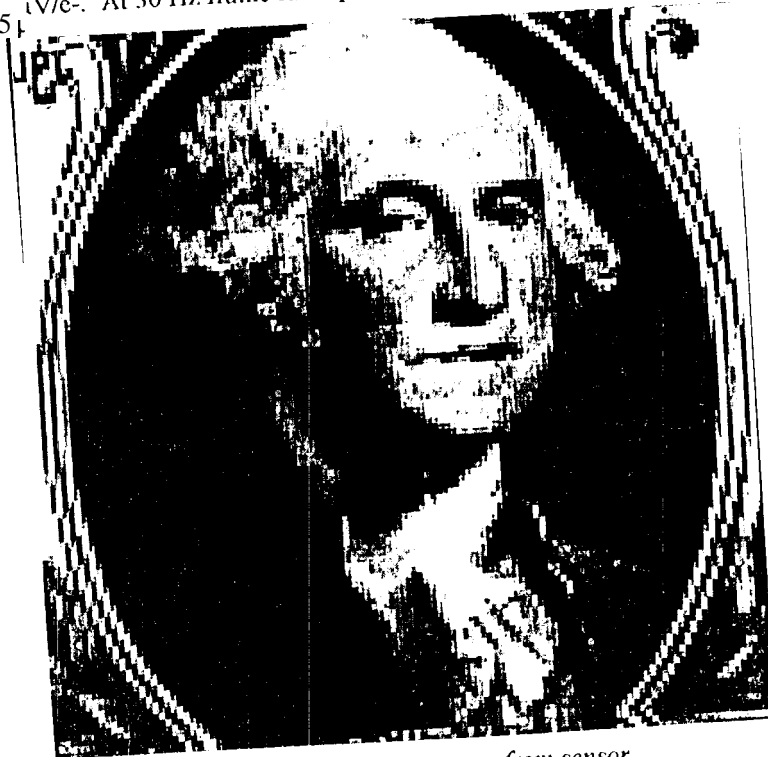


Figure 7. Sample raw image from sensor.

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The quantum efficiency of the detector was measured using a CVI 1/4 m monochromator and a tungsten/halogen light source, calibrated using a photodiode traceable to NIST standards. The quantum efficiency of a pixel is shown below in fig. 7. Peak quantum efficiency exceeds the designed fill factor of the pixel, suggesting that significant optical response is obtained from regions with active readout transistors. Thus the effective fill factor of the pixel is higher than what might be determined from the active area layout alone.

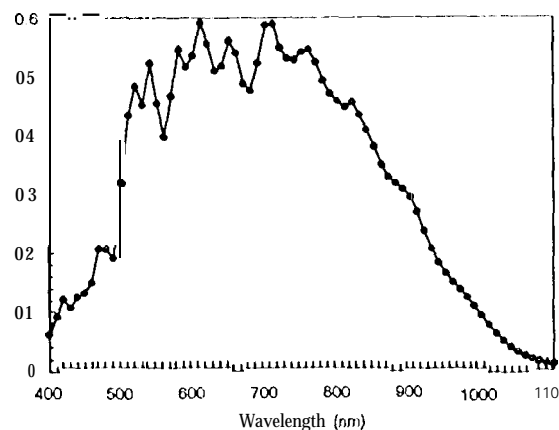


Figure 7. Absolute quantum efficiency of sensor.

It is postulated that the reset noise is equal to the square root of the number of signal carriers detected between the two sampling operations, since this is the number of carriers thermally emitted. The price of this "low noise" reset is image lag. No significant lag was observed, but any such lag is expected to be observed only under extreme conditions.

Noise in the chip was measured by sampling a small window at 100 kpixels/sec. Data was taken by a 16-bit analog-to-digital converter card in a PC workstation. Noise was calculated from the variance in the pixel output signal over 1000 frames of data. Smaller window sizes resulted in faster effective frame rates and lower dark signal levels. Noise measured in the signal dropped well below the theoretical kTC noise level of approximately  $300 \mu\text{V r.m.s.}$  and was limited by the current system noise floor of  $65 \mu\text{V r.m.s.}$  It is thought that because the reset gate voltage levels do not allow reversible transport between the drain and the photodiode, kTC noise is suppressed. With no light and low dark current, the photodiode potential drops below the reset gate surface potential with each succeeding reset due to subthreshold current so that full kTC noise does not develop on the node. For small signals, then, the noise is reflected in the uncertainty in the number of carriers emitted over the reset gate potential barrier. Since this is a thermal emission process, it

Table 2. Performance Characteristics

Parameter	5 Volt Operation		3 Volt Operation	
Saturation level	1300 mV	370,000 e <sup>-</sup>	500 mV	142,000 e <sup>-</sup>
Conversion gain	3.5 $\mu\text{V/e}^-$		3.5 $\mu\text{V/e}^-$	
Read Noise	$\ll 300 \mu\text{V}$	$\ll 86 \text{ e}^-$		
Power			13.8 mW	
Peak QE	~60 %			
Fixed Pattern Noise	$< 2 \text{ mV p-p}$	$< 0.15\%$ @ sat		
Dark Current	15 mV/sec	$< 200 \text{ pA/cm}^2$	5 mV/sec	$< 66 \text{ nA/cm}^2$

## 5. SUMMARY

A CMOS APS chip has been designed that integrates the image sensor technology with digital control functions on a single chip. This has demonstrated the viability of producing a camera-on-a-chip suitable for both commercial, military and scientific applications such as would be encountered in space. The chip has a single clock and single power supply with a simple digital interface that permits easy restructuring of window sizes-of-interest and integration times. The measured performance indicates that this technology will become competitive with CCD's in many applications, resulting in higher overall performance and reduced cost.

Additional work is in progress for integrating the ADC function on-chip<sup>5,6,7</sup>, resulting in all-digital output. Other functions such as automatic exposure and electronic shutter are planned to be integrated in subsequent designs as well. We expect that in the next two to three years we will demonstrate all-digital chips with array sizes up to  $1024 \times 1024$  with pixel sizes in the  $10 \mu\text{m}$  range. Although this paper describes a photodiode APS, there are photogate versions of the APS that are being implemented that offer additional improvements in noise at the tradeoff of quantum efficiency<sup>8</sup>.

## 6. ACKNOWLEDGMENTS

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